UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/699,537	10/30/00	MODEN W	2687.30US (9

MMC1/0517

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EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 05/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/699,537	MODEN, WALTER L.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 1, 8, 26 and 33 are objected to because of the following informalities: There is no antecedent basis in the claims for "the board". For purposes of this office action we will consider the board to be "the substrate". Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 17, 20, 42 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear how a wire that connects a bond pad on a semiconductor die mounted on a die side surface of a board to a bond pad that is also on a die side of the board extends through the board. It is not clear how or why the wire has to extend through a via in the board if both the die and the bond pad on the board to which the die is connected by the wire are both on the same side of the board.

3. Claims 20 and 45 recite the limitation "the... bond pads located on the second attachment surface" in the fourth part of the respective claim. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this office action the bond pads will be considered to be located on the die side surface of the board.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 16 and 26 – 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (USPAT 5674785, Akram) in view of Kohno et al. (USPAT 5293068, Kohno).

Akram discloses in figures 5 – 6 a method of electrically connecting a semiconductor die to a substrate.

With regard to claim 1, Akram discloses in figures 5 – 6 providing a semiconductor die (18) having a surface having a plurality of bond pads thereon (24). Akram discloses in figures 5 – 6 providing a substrate (12b and 12c) having a die side surface, a second attachment surface, at least one via (20b) extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (14), and a plurality of connection points located on the second attachment surface of the substrate. Akram discloses in figures 5 – 6 attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of the substrate. Akram discloses in figures 5 – 6 connecting the plurality of bond pads of the semiconductor die to the plurality of connection points of the substrate using a plurality of wire bonds (32), the plurality of wire bonds extending through the at least one via extending through the substrate. Akram does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the

bond pads of Kohno as the connection points of Akram in order to have a dedicated surface in which to bond a wire to as is well known in the art.

With regard to claim 2, it is inherent in the method of Akram that an adhesive is applied to a portion of the die side of the substrate to attach the semiconductor die thereto.

With regard to claim 3, Akram discloses in figure 6 filling at least a portion of the via in the substrate with a sealant (36b).

With regard to claim 4, Akram discloses in figure 6 filling the via in the substrate with a sealant (36b).

With regard to claim 5, Akram discloses in figures 1 and 3a providing a semiconductor die (18) having a plurality of bond pads (24) thereon. Akram discloses in figure 1 providing a master board (30) inherently having a plurality of circuit traces thereon. Akram discloses in figure 1 providing a board (12) having a die side surface, a second attachment surface, at least one via (20) extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of connection points located on the second attachment surface of the board. Akram discloses in figure 1 providing a plurality of electrical connectors (16) for connecting the plurality of connection points located on the second attachment surface of the board to the circuit traces of the master board. Akram discloses in figure 1 attaching the semiconductor die to a portion of the die side surface of the board. Akram discloses in figure 2 connecting the plurality of bond pads of the semiconductor die to the plurality of connection points of the board using a plurality of wire bonds, the plurality of wire bonds extending through the at least one via extending through then board. Akram discloses in figure 3a connecting the board and master board using the plurality of electrical connectors on

the board to the plurality of circuit traces on the master board. Akram does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Akram in order to have a dedicated surface in which to bond a wire to as is well known in the art.

With regard to claim 6, Akram discloses in figure 1a that the board could include a plurality of vias extending therethrough.

With regard to claim 7, Akram discloses in figure 1 that the plurality of electrical connectors comprise solder balls.

With regard to claim 8, Akram discloses in figure 9 a method of electrically connecting at least two semiconductor die to a substrate. Akram discloses in figure 9 providing at least two semiconductor die (18), each semiconductor die having a surface inherently having a plurality of bond pads. Akram discloses in figure 9 providing a substrate (12m) having a die side surface, a second attachment surface, at least tow vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (14), and a plurality of connection points located on the second attachment surface of the board. Akram discloses in figure 9 attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate. Akram discloses in figure 9 connecting the plurality of bond pads of the semiconductor die to the plurality of connection points of the substrate using a plurality of wire bonds, the plurality of wire bonds extending through the one via extending through the substrate of the at

least two vias extending through the substrate. Akram does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Akram in order to have a dedicated surface in which to bond a wire to as is well known in the art.

With regard to claim 9, it is inherent that Akram applies an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto.

With regard to claims 10 and 11, Akram does not show a sealant in the vias of the embodiment discloses in figure 9. Akram does show a sealant filling the vias in the embodiment shown in figure 6. It is obvious that Akram could fill a portion or all of each via in the substrate with a sealant as done in the embodiment disclosed in figure 6 in order to secure the wires of the embodiment in claim 9 and make the package more durable.

With regard to claim 12, similar to the embodiments disclosed by Akram as applied to claim 8 above, Akram does not disclose a master board in figure 9. Akram does disclose attaching a semiconductor die to a master board in figure 3a and similar to the rejection of claim 5 above. It would have been obvious to one of ordinary skill in the art that electrical connectors (16) shown in figure 9 are used for connecting the plurality of semiconductor die to a master board as shown in figure 3a of Akram.

With regard to claim 13, Akram discloses in figure 9 that the plurality of electrical connectors comprise solder balls.

With regard to claim 14, Akram does not disclose that the plurality of electrical connectors comprise pins. Pins are well known in the art. It would have been obvious to one of

ordinary skill in the art at the time of the present invention to use pins to connect the plurality of semiconductor die to a master board of Akram in order to make an electrical connection between the die and board as is well known in the art.

With regard to claims 15 and 16, they are rejected similar to claims 10 and 11.

Claims 26 – 41 are rejected similar to claims 1 – 16 respectively since the use of the term "at least one" is covered under the definition of "a plurality".

6. Claims 17, 19, 42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (USPAT 6013948, $Akram_1$) in view of Kohno.

As best the examiner can ascertain, $Akram_1$ discloses in figure 4 a method of electrically connecting a semiconductor die (14) to a master board.

With regard to claim 17, $Akram_1$ discloses in figure 1 providing a semiconductor die (14) having a plurality of bond pads (24) thereon. $Akram_1$ discloses in figure 4 providing a master board (10a) inherently having a plurality of circuit traces thereon. $Akram_1$ discloses in figure 4 providing a board (10b) having a die side surface, a second attachment surface , at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads (36b) located on the die side surface of the board. $Akram_1$ discloses in figure 4 providing a plurality of electrical connectors (38a) for connecting the plurality of bond pads located on the die side surface of the board to the circuit traces of the master board. $Akram_1$ discloses if figure 4 attaching the semiconductor die to a portion of the die side surface of the board. $Akram_1$ discloses in figure 4 connecting the plurality of bond pads of the semiconductor die to a plurality of connection points of the board using a plurality of wire bonds, the plurality of wire bonds extending through the at least one via

extending through then board. Akram$_1$ discloses in figure 4 connecting the board and master board using the plurality of electrical connectors on the board to the plurality of circuit traces on the master board. Akram$_1$ does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Akram$_1$ in order to have a dedicated surface in which to bond a wire to as is well known in the art.

With regard to claim 19, Akram$_1$ and Kohno do not disclose that the plurality of electrical connectors comprise wire bonds. Wire bonds are well known in the art. It would have been obvious to one of ordinary skill in the art to use wire bonds as the electrical connectors of Akram$_1$ and Kohno in order to provide a low resistance electrical path from the board to the master board as is well known in the art.

Claims 42 and 44 are rejected similar to claims 17 and 19 respectively since the use of the term "at least one" is covered under the definition of "a plurality".

7. Claims 18 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram$_1$ and Kohno as applied to claim 17 and 42 above, and further in view of Akram.

With regard to claim 18, Akram$_1$ and Kohno do not disclose that the board has a plurality of vias extending therethrough. Akram discloses in figure 1a a board with a plurality of vias (20c) extending therethrough. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the plurality of vias of Akram in the method of Akram$_1$

and Kohno in order to accommodate bond pad configurations for different sizes or types of die as stated in Akram in column 4, lines 50 – 52.

Claim 43 is rejected similar to claim 18 since the use of the term "at least one" is covered under the definition of "a plurality".

8. Claims 20 – 25 and 45 – 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of $Akram_1$ and Kohno.

With regard to claim 20, as best the examiner can ascertain, similar to claim 12 above Akram and Kohno disclose a method of electrically connecting a plurality of semiconductor die to a mater board. Akram and Kohno do not disclose a board with a plurality of bond pads located on the die side surface of the board. $Akram_1$ discloses in figure 4 a plurality of bond pads (36b) located on a die side surface of a board (10b). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads on a die side surface of a board of $Akram_1$ in the method of Akram and Kohno in order to connect a plurality of boards and master boards together as shown by $Akram_1$ in figure 4.

With regard 21, $Akram_1$, Kohno and Akram do not disclose that the plurality of electrical connectors comprise wire bonds. Wire bonds are well known in the art. It would have been obvious to one of ordinary skill in the art to use wire bonds as the electrical connectors of $Akram_1$, Kohno and Akram in order to provide a low resistance electrical path from the board to the master board as is well known in the art.

With regard to claim 22, $Akram_1$, Kohno and Akram does not disclose that the plurality of electrical connectors comprise pins. Pins are well known in the art. It would have been

obvious to one of ordinary skill in the art at the time of the present invention to use pins to connect the plurality of semiconductor die to a master board of $Akram_1$, Kohno and Akram in order to make an electrical connection between the die and board as is well known in the art.

With regard to claims 23 and 24, they are rejected similar to claims 10 and 11.

With regard to claim 25, it is inherent that Akram applies an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto.

Claims 45 – 50 are rejected similar to claims 20 – 25 respectively since the use of the term "at least one" is covered under the definition of "a plurality".

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oshima et al., Farnworth et al., Matsura et al., Sato et al., Tsubosaki et al., Lim et al., Shen and Conru et al. all disclose a semiconductor die mounted to a substrate with vias extending through the substrate and wires in the vias connecting the die to the opposite side of the substrate from which it is mounted.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
May 10, 2001

EDDIE LEE
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